What is claimed is:

1. A method for fabricating a ferroelectric random access memory device, comprising the steps of:

(a) forming a first inter-layer insulation layer on a substrate providing a transistor;

(b) etching the first inter-layer insulation layer to form a storage node contact hole exposing a partial portion of the substrate;

(c) burying a storage node contact including a plug and a barrier metal layer into the storage node contact hole;

(d) forming an adhesion layer on the storage node contact and the first inter-layer insulation layer;

(e) inducing a predetermined portion of the adhesion layer to be cracked, the predetermined portion disposed above an upper part of the plug;

(f) selectively removing the cracked predetermined portion to expose a surface of the barrier metal layer formed on the plug; and

(g) forming a ferroelectric capacitor connected to the plug through the exposed surface of the barrier metal layer.

2. The method as recited in claim 1, wherein the plug is made of a conductive material having a thermal expansion coefficient greater than that of the first inter-layer insulation layer.

3. The method as recited in claim 2, wherein the first inter-layer insulation layer is made of a silicon oxide-based material and the plug is formed with one of polysilicon or tungsten.

4. The method as recited in claim 1, wherein at the step (e), the crack is induced by performing a rapid thermal annealing process.

5. The method as recited in claim 4, wherein the rapid thermal annealing process proceeds at a temperature ranging from about 400 °C to about 1000 °C in an atmosphere of nitrogen (N_2) or argon (Ar) gas.

6. The method as recited in claim 1, wherein the step (f) includes a cleaning process carried out for about 1 minute to about 60 minutes with use of one of a chemical solution SC-1 obtained by mixing ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and water (H_2O) in a ratio of about 1 to about 4 to about 20 and a sulfuric acid-peroxide mixture (SPM) solution which is a mixture of H_2SO_4 and H_2O_2.

7. The method as recited in claim 1, wherein the adhesion layer is made of alumina (Al_2O_3), titanium oxide (TiO_2) and tantalum oxide (TaO_2).

8. The method as recited in claim 1, wherein the

adhesion layer has a thickness ranging from about 10 Å to about 500 Å.

9. The method as recited in claim 1, wherein the step (g) includes the steps of:

forming a conductive layer for use in a bottom electrode on a structure including the exposed barrier metal layer and the adhesion layer;

forming the bottom electrode by etching the conductive layer and the adhesion layer;

forming a second inter-layer insulation layer having a planarized upper surface and encompassing the lower electrode;

forming a ferroelectric layer on the bottom electrode and the second inter-layer insulation layer; and

forming an upper electrode on the ferroelectric layer.

10. The method as recited in claim 1, wherein the step (g) includes the steps of:

forming a first layer for use in a bottom electrode on a structure including the exposed barrier metal layer and the adhesion layer;

etching the first layer and the adhesion layer to form a first stack structure;

forming a second inter-layer insulation layer having a planarized upper surface and encompassing the first stack structure;

sequentially forming a second layer for use in the

bottom electrode and a ferroelectric layer on the first stack structure and the second inter-layer insulation layer;

etching the ferroelectric layer and the second layer to form a second stack structure;

forming a third inter-layer insulation layer having a planarized upper surface and encompassing the second stack structure; and

forming an upper electrode on the ferroelectric layer.

11. The method as recited in claim 10, wherein the step of performing a thermal process for crystallizing the ferroelectric layer and removing impurities proceeds before or after the step of forming the upper electrode.

12. The method as recited in claim 10, wherein the first layer is made of a material selected from a group consisting of iridium (Ir), ruthenium titanium nitride (RuTiN), chromium tantalum nitride (CrTaN), chromium titanium nitride (CrTiN) and ruthenium tantalum nitride (RuTaN) and the second layer is formed by stacking a platinum (Pt) layer and an iridium oxide (IrO_2) layer.

13. The method as recited in claim 9, wherein the second inter-layer insulation layer includes double layers having an oxygen barrier layer made of a material selected from a group consisting of alumina (Al_2O_3), silicon nitride (Si_3N_4) and silicon oxynitride (SiON) and an insulation layer

made of a material selected from a group consisting of high density plasma (HDP) oxide, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), middle temperature oxide (MTO), high temperature oxide (HTO) and tetraethylorthosilicate (TEOS) oxide or in a single layer including the insulation layer.

14. The method as recited in claim 10, wherein the second inter-layer insulation layer includes double layers having an oxygen barrier layer made of a material selected from a group consisting of Al_2O_3, Si_3N_4 and SiON and an insulation layer made of a material selected from a group consisting of HDP oxide, BPSG, PSG, MTO, HTO and TEOS oxide or in a single layer including the insulation layer.

15. The method as recited in claim 10, wherein the third inter-layer insulation layer includes double layers having an oxygen barrier layer made of a material selected from a group consisting of Al_2O_3, Si_3N_4 and SiON and an insulation layer made of a material selected from a group consisting of HDP oxide, BPSG, PSG, MTO, HTO and TEOS oxide or in a single layer including the insulation layer.